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DATE OF BIRTH:
November 3, 1943

EDUCATION:
- Ph.D (Computer Science), **University of Waterloo**, Waterloo, Ontario, 1971.
- M.Sc (Electrical Engineering), **University of Ottawa**, Ottawa, Ontario, 1967.
- B.Tech (Electrical Engineering), **Indian Institute of Technology, Kanpur**, 1965.

INDUSTRIAL EXPERIENCE:
- Member, Scientific Staff, **Bell-Northern Research** (now Nortel Networks), Toronto, July 1970- August 1971.
- Member, Scientific Staff, **Northern Electric Research Laboratories** (now Nortel Networks), Toronto, May-August, 1967.

ACADEMIC EXPERIENCE:

- **Professor**, Department of Computing & Information Science, University of Guelph, Guelph, Ontario, 1983 to present.
- **Professor & Dean**, School of Computer and Systems Sciences, Jawaharlal Nehru University, New Delhi, 1978-1983.
- **Visiting Professor**, Department of Computing & Information Science, University of Guelph, Guelph, Ontario, 1980-1981.
- **Assistant/Associate Professor**, Department of Computer Science, University of Ottawa, Ottawa, Ontario, 1971-1978. (contd.)….

•**Course Director**, Department of Computer Science, York University, Toronto, Ontario, Summer 1971.
•**Lecturer**, Department of Applied Analysis & Computer Science, University of Waterloo, Waterloo, Ontario, 1968-1969.

CURRENT RESEARCH INTERESTS:

VLSI Design Automation, Field Programmable Gate Array (FPGA) CAD Tools and Algorithms

PUBLICATIONS:

A) BOOK

D.K. Banerji & J. Raymond, **Elements of Microprogramming**, Prentice-Hall, Inc., Englewood Cliffs, N.J., 1982, 434 pages.

B) BOOK CHAPTER

Wilson, T.C., G. Grewal, S. Henshall, and D.K. Banerji, "An ILP-based Approach to Code Generation", in **Code Generation for Embedded Processors,** Peter Marwedel and Gert Goossens (eds.), Kluwer Academic Publishers, Boston, Ma., June 1995, pp. 103-118 (Initial version presented at the **First European Workshop on Code Generation for Embedded Processors,** Dagstuhl, Germany, August '94).

C) ARTICLES SUBMITTED

Banerji, D.K., Gary Grewal, and Zhibin Dai,"Routability Prediction for FPGAs based on a Routing Hierarchy", **communicated,** January 2007.

D) ARTICLES IN REFEREED JOURNALS (in reverse chronological order)

[1] Grewal, G., S. Coros, A. Morton, and D. Banerji, "Assigning Data to Dual Memory Banks in DSPs with a Genetic Algorithm using a Repair Heuristic," accepted to appear in the **Journal of Applied Intelligence**, Springer, 2006, 23 pages.

[2] Areibi, S., G. Grewal, D. Banerji, and P. Du, "Hierarchical FPGA Placement," accepted for **IEEE Canadian Journal of Electrical and Computer Engineering,** 2006, 26 pages.

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[9] Wilson, T.C., D.K. Banerji, A. Basu, J.C. Majithia, and A.K. Majumdar, "Port Assignment in Multiport Memories for Interconnection Minimization in Datapath Synthesis", **Logic and Architecture Synthesis**, P. Michel and G. Saucier (eds.), Elsevier Science Publishers B. V. (North Holland), IFIP, 1991, pp. 59-68.

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Also reprinted in **IEEE Tutorial on Distributed Computing, 1978** and in **IEEE Tutorial on Distributed Computing: An Overview, 1981.**

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E) TECHNICAL CONFERENCE PUBLICATIONS (in reverse chronological order)

[1] Grewal, G., Stelian Coros, Dilip K. Banerji, Andrew Morton, and Mario Ventresca, "Optimized Memory Assignment for DSPs", **IEEE World Congress on Computational Intelligence,** Vancouver, BC, July 2006.

[2] Chowdhury, S., G. Grewal, and D. Banerji, "Clustering Hanan Points to Reduce VLSI Interconnect Routing Times," **Proc. IEEE Canadian Conference on Electrical & Computer Engineering**, Ottawa, May 7-10, 2006, 5 pages.

[3] Grewal, G., S. Coros, A. Morton, and D. Banerji, "A Multi-objective Integer-Linear Programming Model for Assigning Data to Memory in the DSP Domain," **IEEE Workshop on Memory Performance Issues,** Austin, Texas, February 2006.

[4] Grewal**,** G., S. Coros, D. Banerji, and A. Morton, "Comparing a Genetic Algorithm Repair Heuristic and Penalty Function in the DSP Domain," **International Conference on Artificial Intelligence and Applications***,* Innsbruck, Austria, February 2006, 10 pages.

[5] Grewal, G., S. Coros, A. Morton, and D. Banerji, "An Evolutionary Penalty-Function Approach to Memory Assignment in the DSP Domain," **10th IEEE Annual Workshop on Interaction between Compilers and Computer Architectures**, Austin, Texas, February 2006.

[6] Du, Peng, Gary Grewal, Shawki Areibi, and D.K. Banerji," A Fast Hierarchical Approach to FPGA Placement", **Proceedings of the International Conference on VLSI,** Las Vegas, June 2004, pp. 497-503.

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[9] Dai, Zhibin, and D.K. Banerji,"Routability Prediction for Field-Programmable Gate Arrays with a Routing Hierarchy", **Proceedings of Sixteenth IEEE International Conference on VLSI Design,** New Delhi, January 2003, pp. 85-90.

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[18] Wilson, T.C., M. Garg, R. Deadman, B. Halley, and D.K. Banerji, "MinMux: A New Approach for Global Minimization of Multiplexers in Interconnect Synthesis," **3rd Great Lakes Symp. on VLSI,** Kalamazoo, Mi., March 1993, pp. 132-138.

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[20] Wilson, T.C., B. Halley, R. Deadman, and D.K. Banerji, "Optimal Register Allocation and Binding in Behavioral Synthesis", **Proc. CCVLSI 1992**, Halifax, N.S., October, 1992, pp. 108-115.

[21] Basu, A., D.K. Banerji, T.C. Wilson, and J.C. Majithia, "An Approach to Minimize Testability Overhead for BILBO-based Built-in-Self-Test", **VLSI Design 1992, Fifth International Conf. on VLSI Design**, Bangalore, India, January 1992.

[22] Wilson, T.C., Anupam Basu, D.K. Banerji, and J.C. Majithia, "Interconnect Optimization through Commutative Input Pair Alignment", **Canadian Conference on VLSI 91**, August 1991, Kingston, Ontario, pp. 4B.4.1-4B.4.8.

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[33] Balakrishnan, M., A.K. Majumdar, D.K. Banerji, and J.G. Linders,"Synthesis of Decentralized Controllers Using Control Graph Partitioning", **Proceedings of 30th Midwest Symposium on Circuits and Systems,** Syracuse, NY., August 1987, pp. 591-594.

[34] Balakrishnan, M., S. Sutarwala, A.K. Majumdar, D.K. Banerji, J.G. Linders, and J.C. Majithia, "A Semantic Approach for Modular Synthesis of VLSI Systems", **Proceedings of IASTED International Conference,** Paris, June 1987, pp. 66-69.

[35] Linders, J.G., M. Balakrishnan, A.K. Majumdar, D.K. Banerji, and J.C. Majithia, "A Modular Synthesis Technique for Automated VLSI Design", **Proceedings of COMPEURO '87: VLSI and Computers,** Hamburg, May 1987, pp. 262-267.

[36] Jha, A.C., S.P. Rana and D.K. Banerji, "Realizable Decentralized Control for Distributed Computing Systems", **27th Technical Convention of the Institute of Electronics & Telecom Engineers,** New Delhi, February 1984.

[37] Jha, A.C., S. P. Rana and D.K. Banerji,"On Realizable Strategies for Distributed Sensor Network Systems", **Seminar on Signal Processing, Naval Physical and Oceanographic Laboratory,** Defense Research & Development Organization, Cochin, India, November 1983.

[38] Banerji, D.K. and S. Kaushik,"Representation and Processing of Fractions in a Residue System", **Sixth IEEE Symposium on Computer Arithmetic,** University of Aarhus, Aarhus, Denmark, June 1983.

[39] Jha, A.C. & D.K. Banerji, "On Realizable Strategies for Distributed Problem Solving", **1983 Conference of Computer Society of India,** Ahmedabad, India, February 1983, pp.A2.18.01-08.

[40] Banerji, D.K., To-Yat Cheung, and V. Ganesan, "A High-Speed Division Method in Residue Arithmetic", **Fifth IEEE Symposium on Computer Arithmetic,** University of Michigan, Ann Arbor, Mi., May 1981, pp. 158-164.

[41] Churchill, P., J. Raymond, and D.K. Banerji, "Assistance de Systemes d'Exploitation par la Microprogammation", **46eme Congres de l'ACFAS,** Ottawa, May 1978.

[42] Banerji, D.K., S.C. Hung, J. Raymond and G.M. White, "A NOVA Emulator on the Microdata 1600", **MIMI '77,** Zurich, June 1977.

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[44] Banerji, D.K., "On Combinational Logic for Sign Detection in Residue Number Systems", **Third IEEE Symp. on Computer Arithmetic,** Southern Methodist University, Dallas, Texas, November 1975 , pp. 113-116.

[45] Banerji, D.K. & J. Raymond, "Microprocessor and Floppy Disk Get Together for Low-cost Text Editing", **MIMI '75 ,** Zurich, June 1975, pp. 284-285.

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[48] Raymond, J., D.K. Banerji & A. Perez, "Considerations sur l'implementation d'un logiciel d'exploitation microprogramme", **43e congres de l'ACFAS,** Universite de Moncton, May 1975.

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[50] Banerji, D.K., Z. Krokar, & J. Raymond, "Design of a Microprocessor Based Text Editing System", **Symposium on Circuits, Systems and Computers,** University of Calcutta, February 1975.

[51] Raymond, J., J-C. Gavrel & D.K. Banerji, "L'utilisation d'un microprocesseur pour realiser un systeme graphique intelligent", **Journees d'electronique 74 (International Conference on Microprocessors),** Lausanne, Switzerland, October 1974, pp. 233-240.

[52] Banerji, D.K. and J. Raymond, "A Cross Assembler and Interpreter for INTEL 8008 Microprocessor", **Journees d'electronique 74 (International Conference on Microprocessors),** Lausanne, Switzerland, October 1974, pp 177-182.

[53] Das, S.R. & D.K. Banerji, "On Control Memory Minimization in Microprogrammed Digital Computers", **Sixth Asilomar Conference on Circuits and Systems,** Pacific Grove, California, November 1972, pp. 174-178.

[54] Banerji, D.K., "A Novel Implementation Method for Addition and Subtraction in Residue Number Systems", **IEEE Symposium on Computer Arithmetic,** University of Maryland, College Park, Maryland, May 1972.

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F) NON-REFEREED CONTRIBUTIONS

Technical Reports

[1] Wilson, T.C., M.K. Garg, R. Deadman, B. Halley, and D.K. Banerji, "Global Optimization of Multiplexers and Buses in Interconnect Synthesis", **Tech. Report # CIS93D1,** Dept. of Computing & Information Science, University of Guelph, Ontario, January 1993.

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[3] Wilson, T.C., D.K. Banerji, and Anupam Basu, "Reducing Interconnections through Register Role Alignment", **Tech. Report #CIS90D6**, Dept. of Computing & Information Science, University of Guelph, Guelph, Ontario, April 1990.

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Theses

[1] Banerji, D.K.,"Residue Arithmetic in Computer Design", **Ph.D. thesis**, Dept. of Computer Science, University of Waterloo, March 1971.

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G) INVITED TALKS

[1] Banerji, D.K.," A Fast Heuristic for FPGA Placement", **School of Computer & Systems Sciences,** Jawaharlal Nehru University, New Delhi, February 2004.
Also presented at the **Department of Computer Science & Engineering,** Indian Institute of Technology, Kanpur, March 2004.

[2] Banerji, D.K.," Routability Prediction for Hierarchical FPGAs with Mixed Routing Resources", **School of Computer & Systems Sciences,** Jawaharlal Nehru University, New Delhi, February 2004.

[3] Banerji, D.K.," CAD for VLSI", **Workshop on VLSI: Recent Trends and Challenges**, Delhi College of Engineering, University of Delhi, March 2004.

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[18] Ahmad, S.I. & D.K. Banerji, "Developments in Minicomputer Architecture", **CIPS Technical Meeting, Bell-Northern Research,** Ottawa, January 1973.

THESES SUPERVISED AT THE UNIVERSITY OF GUELPH:

The following theses in VLSI and FPGA CAD areas have been supervised/co-supervised in the Department of Computing & Information Science, University of Guelph:

[1] Chowdhury, S, **Efficient Steiner Tree Construction based on Clustering of Hanan Points,** May 2005 (joint supervision with Gary Grewal).

[2] Perera, Keerthi, **An Efficient Caching Strategy for Web Services,** December 2003.

[3] Du, Peng, **A Fast Heuristic Technique for FPGA Placement based on Multilevel Clustering,** December 2003 (joint supervision with Gary Grewal) .

[4] Chen, Jian, **Routability Prediction for Field Programmable Gate Arrays with Mixed Routing Resources,** August 2003.

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[19] Basu, Amit, **Insertion of Testability Hardware into Synthesized Datapaths**, May 1990 (jointly supervised with T. C. Wilson).

[20] Sutarwala, Shailesh, **High-Level Synthesis of Datapaths from Behavioral Descriptions,** May 1988(jointly supervised with A.K. Majumdar).

COURSES TAUGHT:

University of Guelph
•CIS100 Introduction to Computing
•CIS150 Introduction to Programming Techniques
•CIS202 Introduction to Computer Organization
•CIS312 Digital Systems
•CIS346 System Simulation
•CIS405 Advanced Computer Architecture
•CIS450 Special Topics in Computer Science
•CIS620 Design Automation in Digital Systems

Jawaharlal Nehru University, New Delhi
•Computer Architecture
•Mini & Micro Computer Systems

University of Ottawa
•CSI 1100 Computing Concepts and Programming I
•CSI 2116 Introduction to Computer Organization
•CSI 2140 Programming Language Instruction
•CSI 2150 Computational Methods in Numerical Problems
•MAT 2280 Numerical Methods
•CSI 3116 Computer Organization
•CSI 3400 Computer Science Laboratory

•CSI 4103 Topics in Computer Science I
•CSI 4114 (ELG 5189) Microprogramming & Machine Architecture
•CSI 4201 Topics in Computer Science

York University
•Computer Organization

University of Waterloo
•Switching Theory
•Non-numeric Computation

OTHER PROFESSIONAL ACTIVITIES:

a) Refereeing

- IEEE Transactions on Computers
- IEEE Transactions on CAD
- Prentice-Hall, Inc., (book manuscripts)
- NSERC (Canada) and NSF (USA) grant applications
- Computer Architecture Conferences
- IEEE Conferences on Computer Arithmetic
- International Journal of Computer-Aided VLSI Design
- Journal of the Institute of Electronics & Telecom Engineers, New Delhi
- International Conf. on VLSI Design
- VLSI Design journal
- Canadian Conf. on VLSI (CCVLSI)
- Ninth International Parallel Processing Symposium (1995)

b) Program Committee Member

- International Conf. on VLSI Design
- Sixth IEEE Symposium on Computer Arithmetic, Aarhus, Denmark, June 1983
- Fifth IEEE Symposium on Computer Arithmetic, Ann Arbor, Mi., May 1981
- MIMI (International Conf. on Mini and Micro Computers), Zurich 1979 and Toronto 1976

c) Consulting

- Digital Electronic Laboratories, Ottawa, 1976-80
- Data General Corporation, Southboro, Mass., 1977

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